WHAT IS CLAIMED IS:

1. A semiconductor device, comprising:

a fin structure comprising a semiconducting material, the fin structure including an insulating layer;

a source region formed at one end of the fin structure and including the insulating layer, the insulating layer separating the source region into a first source region and second source region;

a drain region formed at an opposite end of the fin structure and including the insulating layer, the insulating layer separating the drain region into a first drain region and second drain region; and

at least one gate.

2. The semiconductor device of claim 1 wherein a width of the insulating layer ranges from about 20 Å to about 30 Å.

3. The semiconductor device of claim 1 wherein the first source region and the first drain region are formed on a first side of the insulating layer and the second source region and the second drain region are formed on an opposite side of the insulating layer.

4. The semiconductor device of claim 3 wherein the first source region and the first drain region are part of an N-channel device, and

wherein the second source region and the second drain region are part of a P-channel device.

5. The semiconductor device of claim 1 wherein each of the N-channel device and the P-channel device includes the at least one gate.

6. The semiconductor device of claim 1 wherein the insulating layer comprises an oxide.

7. The semiconductor device of claim 1 wherein the insulating layer comprises a high K dielectric.

8. A semiconductor device, comprising:

a fin structure that includes an insulating layer that extends a length of the fin structure and positioned approximately in a center of the fin structure;

a source region formed at one end of the fin structure and including the insulating layer, the insulating layer separating the source region into a first source region and second source region; and

a drain region formed at an opposite end of the fin structure and including the insulating layer, the insulating layer separating the drain region into a first drain region and second drain region.

9. The semiconductor device of claim 8 further comprising at least one gate formed over the fin structure.

10. The semiconductor device of claim 8 wherein a width of the fin structure ranges from about 20 Å to about 30 Å.

11. The semiconductor device of claim 10 wherein a width of the insulating layer ranges from about 20 Å to about 30 Å.

12. The semiconductor device of claim 8 wherein the first source region and the first drain region are formed on a first side of the insulating layer and the second source region and the second drain region are formed on an opposite side of the insulating layer.

13. The semiconductor device of claim 12 wherein the first source region and the first drain region are part of an N-channel device, and

wherein the second source region and the second drain region are part of a P-channel device.

14. The semiconductor device of claim 8 wherein the first source and drain regions are doped with n-type impurities and the second source and drain regions are doped with p-type impurities, and

wherein the semiconductor device further comprising:

a common gate formed on at least a top and one side surface of the fin structure.

15. The semiconductor device of claim 8 wherein the insulating layer comprises a high K material.

16. A semiconductor device comprising:

an N-channel device including a first source region, a first drain region, a first fin structure, and a gate; and

a P-channel device including a second source region, a second drain region, a second fin structure, and the gate, the second source region, the second drain region, and the second fin structure being separated from the first source region, the first drain region, and the first fin structure by an insulating layer.

17. The semiconductor device of claim 16 wherein a width of the insulating layer ranges from about 20 Å to about 30 Å.

18. The semiconductor device of claim 16 wherein the insulating layer comprises an oxide.

19. The semiconductor device of claim 16 wherein the insulating layer comprises a high K material.

20. The semiconductor device of claim 16 wherein a width of each of the first fin structure and the second fin structure ranges from about 20 Å to about 30 Å.